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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,162	12/15/2003	Ji Yong Park	1514.1030	2087

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EXAMINER

LANDAU, MATTHEW C

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/734,162	Applicant(s) PARK ET AL.	
	Examiner Matthew Landau	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 May 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 May 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>5/25/06, 5/31/06</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement filed May 25, 2006 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Drawings

The drawings were received on May 25, 2006. These drawings are unacceptable. Although drawings are not necessarily to scale, the angle of the primary grain boundaries (with respect to the current direction) shown in new Figure 6 is clearly greater than 45 degrees.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the primary crystal grain boundaries are inclined to a current direction between active channel regions of the thin film transistor at an angle of -45° to 45° (in conjunction with the limitations of claim 1) must be shown or the feature(s) canceled from the claim(s). Note that Figure 6 shows the primary grain boundaries inclined to the current direction at an angle of approximately 90 degrees. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet,

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even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5, 6, 11, and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 5, 6, 11, and 12, the limitation “a current direction between active channel regions of the thin film transistor” renders the claim indefinite. It is unclear how a single transistor can have multiple channel regions. Furthermore, it is unclear what direction Applicant is attempting to define by using this limitation. Is the current direction referred to by this

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limitation the horizontal direction between the source and drain (as shown in Figure 6), or is the vertical direction.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4, 7, 8, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Isobe et al. (US Pat. 6,890,840, hereinafter Isobe).

Regarding claim 1, 4, 7, and 10, Figures 1A-1E and 3 of Isobe disclose a thin film transistor (TFT) comprising a lightly doped drain (LDD) region 304 (col. 7, lines 35-40), wherein the TFT is formed so that primary crystal grain boundaries of a polysilicon substrate are not positioned in the LDD region. Isobe disclose the crystal aggregate boundaries are located outside of the TFT formation region (col. 6, lines 29-34). It is considered that the aggregate boundaries are the primary grain boundaries. Since there are no primary grain boundaries in the TFT region, there cannot be any primary grain boundaries in the LDD region. Regarding claims 2, 7, and 10, Isobe further discloses the TFT can be used in an active matrix liquid crystal module (LCD) (col. 15, lines 63-65), which is a flat panel display device.

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Regarding claims 2 and 8, as stated above, Isobe discloses the primary grain boundaries are located outside the TFT formation region (col. 6, lines 29-34). Therefore, a width of the activation layer including the LDD region must be shorter than a distance between the primary grain boundaries.

Claims 1, 4-6, and 10-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (US Pat. 6,720,578)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1, 4, 7, 10, 13, and 14, Figure 8 of Lee discloses a flat panel display (LCD) (see claim 14) comprising: a thin film transistor (TFT) (col. 6, lines 1-3) comprising: an offset region (gate insulator, inherently part of TFT); wherein the thin film transistor is formed so that primary grain boundaries of a polysilicon substrate are positioned in channel, source and drain regions but not positioned in the offset region. The gate insulator can be considered the offset region since it "offsets" the gate from the channel. The claim does not require the "offset region" to be within the polysilicon substrate, but merely requires it to be part of the TFT. A gate insulator is part of a TFT.

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Regarding claims 5 and 11, as best the examiner can ascertain the claim invention, Figure 8 of Lee discloses the primary crystal grain boundaries are perpendicular to a current direction between the active channel regions of the thin film transistor.

Regarding claims 6 and 12, as best the examiner can ascertain the claimed invention, Figure 8 of Lee discloses the primary crystal grain boundaries are inclined to a current direction between active channel regions of the TFT at an angle of -45 degrees to 45 degrees.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al. (US Pat. 5,563,426, hereinafter Zhang) in view of Suzuki et al. (US Pat. 6,274,888, hereinafter Suzuki).

Regarding claims 1, 4, 7, and 10, Figures 1(B), 1(C), and 4(C) disclose a TFT formed so that primary crystal grain boundaries 4 of a polysilicon substrate are formed outside the TFT formation regions. The difference is the TFT comprises an LDD region. Suzuki discloses a TFT comprises an LDD region (col. 7, lines 34-40). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of

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Zhang by including an LDD region for the purpose of reducing short channel effects, which is well-known in the art. Since, as shown in Figure 1(C), the primary grain boundaries are located away from the semiconductor regions 6 that make up the TFTs, the primary grain boundaries cannot be located in the LDD region. Regarding claims 4, 7, and 10, Suzuki further discloses the TFT can be used in a liquid crystal display device (i.e., flat panel device) (col. 16, lines 54-57).

Regarding claims 2 and 8, as stated above, Figure 1(C) of Zhang discloses the primary grain boundaries are located away from the semiconductor regions 6 that make up the TFTs. Therefore, a width of the activation layer including the LDD region must be shorter than a distance between the primary grain boundaries.

Regarding claims 3 and 9, product-by-process limitation “wherein the polysilicon substrate is formed by a sequential lateral solidification (SLS) method” does not patentably distinguish the claimed invention.

Regarding claims 5, 6, 11, and 12, Figure 1(C) of Zhang discloses many different primary grain boundaries. Some extend vertically and some extend horizontally, but all the TFTs shown have current flowing in the same direction. Therefore, Figure 1(C) of Zhang discloses primary grain boundaries that are perpendicular to a current direction between active channel regions of the thin film transistor (claims 5 and 11), as well as primary grain boundaries that are inclined to a current direction between active channel regions of the thin film transistor at an angle of zero degrees (i.e., parallel) (claims 6 and 12).

Response to Arguments

Applicant's arguments filed October 13, 2005 have been fully considered but they are not persuasive.

Applicant argues that the method disclosed by Isobe is an MILC (metal induced lateral crystallization) method, and that a MILC method cannot form primary crystal grain boundaries. However, Applicant has not provided any evidence to support this allegation that primary crystal grain boundaries cannot be formed. Furthermore, it can be considered that the grain boundaries formed in the process of Isobe are in fact "primary" grain boundaries. Applicant has not explicitly defined "primary grain boundaries" in a manner that would preclude this interpretation. Using the broadest reasonable interpretation, if a device has only one type of grain boundary, those boundaries can be considered "primary" grain boundaries. Note that Applicant makes similar arguments regarding the rejection of Zhang in view of Suzuki. Therefore, the above response also applies to those arguments. Further regarding Zhang, the boundaries 4 shown in Figure 1(B) can certainly be considered primary grain boundaries since they are the intersection of different crystal growth regions. In these growth regions, the crystals grow radially outward from the center of the growth regions. Therefore, Applicant's arguments are not persuasive.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

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The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Matthew C. Landau

August 5, 2005